# Overall system architecture

Package in package 'Introduction'

Overall system architecture

Version 1.0 Phase 1.0 Proposed

dong.wu created on 1/31/2018. Last modified 2/9/2018

## system overall architecture diagram

Component diagram in package 'Overall system architecture'

*This is Overall system architecture diagram* use to guide software design, test case design, Function Safety analysis.

System module Definition:

System module is the abstraction and generalization of software module, may no correspond with the software module one by one.

GVP:Communication module, include Autosar Stack and ASAL module, all the public CAN and private CAN signal send out from this module, only receive message from the private CAN, for public CAN need send out the EMS/EPS/ESP/VDM/HMI command.

GVP: VPcommunication, Receive VP message and data of vision , send VP data to IHBC, LANE ,SLIF. send vehicle information to VP.

. System Time: Time from CAN,

system overall architecture

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1. system overall architecture

## Fault Manager diagram

Component diagram in package 'Fault Manager'

This fault manager module is new design base on MVS platform. Fault Manager(FM) is the core SWC to fulfill the fault manager. It is carried over from CADS4. The main function is to set DTC events and switch off features depending on the signals received.

EVTSet port between Fault Manager and DEM is prefer to remove, replace by system alarm port between Fault Manager and MAST, all the DTC information will feed to DEM pass through MAST and MDTC.

Fault Manager

Version 1.0

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1. Fault Manager

Version 1.0 Phase 1.0 Proposed

## Watchdog Manager diagram

Component diagram in package 'Watchdog Manager'

**MCU Core 0:**  Primary core , implement Watchdog Manager, feed extern watchdog

**MCU Core1:** core for Object Fusion, report alive states to Core 0

**MCU Core2:** core for Feature implement, report alive states to Core 0

**Watchdog Manager:** Monitoring MCU core 1 and core 2 alive states, monitoring critical task in core 0, feed internal watchdog, initialize external watchdog.

**Be Monitored Core Task:** critical task which task need to be monitored, this kind of task need report each running states cyclically.

**OS task:** an idle task to report MCU alive states.

**MCU reset:** it's a hardware pin to reset MCU

**Internal watchdog:** Watchdog Manager will feed Internal WD base on the states report of Core 1 Core 2 and critical task in Core 0. if any task stuck, Internal Watchdog will reset MCU.

**VP Watchdog:** VP WD use to monitor VP states, if VP stuck and nor states reported, VP will be reset.

Watchdog Manager

Version 1.0

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1. Watchdog Manager

## Watchdog Manager Sequence diagram

Interaction diagram in package 'Watchdog Manager'

Watchdog Manager Sequence

Version 1.0

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1. Watchdog Manager Sequence